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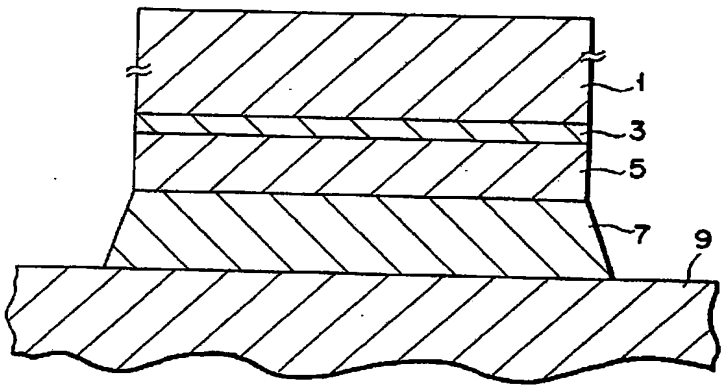
(54) Bonding semiconductor chips to a lead frame

(57) In a semiconductor device a metal layer (3, 5) is deposited on the bottom plane of a semiconductor chip (1). An alloy layer (7) acts as a brazing agent for brazing together the metal layer (3, 5) and a lead frame (9). The alloy layer (7) comprises tin and copper and it may further include antimony, phosphorus and bismuth. The layers 3, 5 are of vanadium and nickel respectively. All the layers may be formed by evaporation, thermal deposition or by plating. A layer of gold may be applied beneath the alloy layer 7.

FIG. 1



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The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

FIG. 1

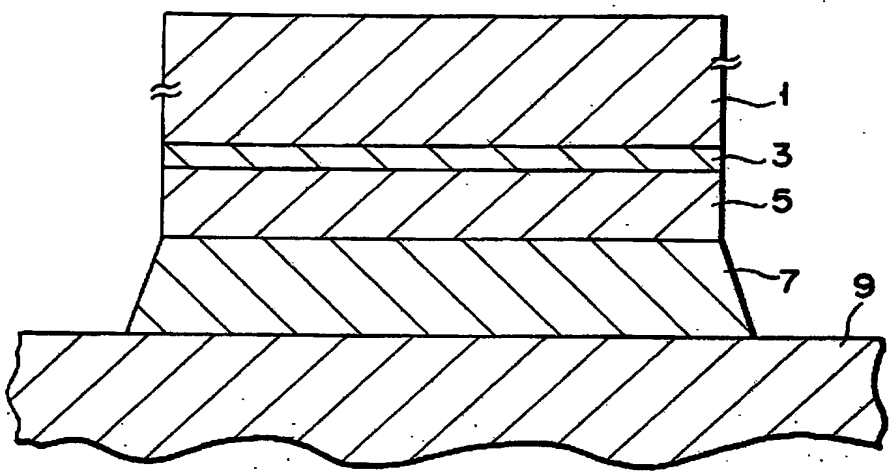


FIG. 2

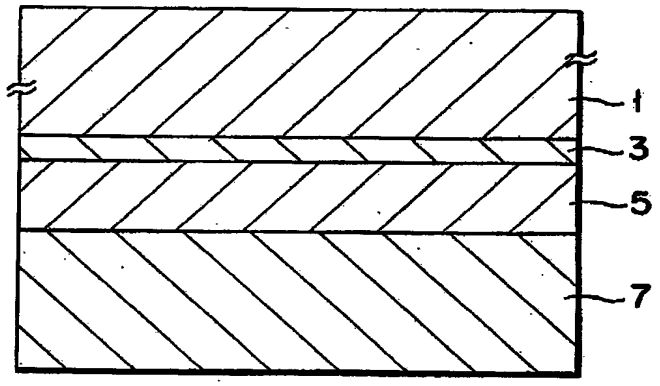
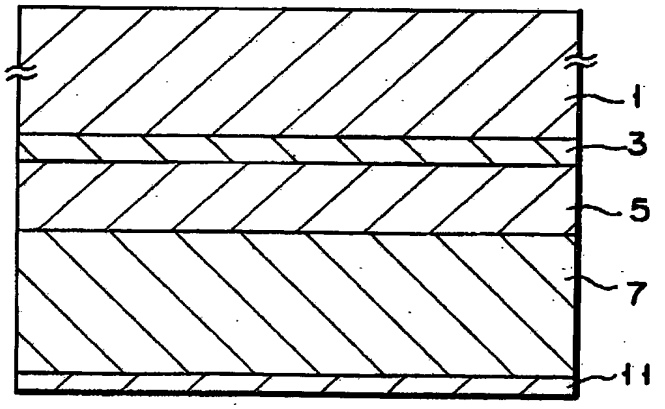


FIG. 3



SPECIFICATION

A semiconductor device

This invention relates to an improvement on a semiconductor device and more particularly to a semiconductor device in which a semiconductor chip and lead frame are bonded together by a brazing agent prepared from an alloy of tin and copper.

Fig. 1 illustrates the construction of a common semiconductor device described, for example, in the Japanese disclosed patent applications No. 55—19805 and No. 55—19806. Referring to the construction of the semiconductor device of Fig. 1, a vanadium layer 3 is deposited on the bottom plane of a semiconductor chip 1. A nickel layer 5 is formed underneath the vanadium layer 3 to prevent the gold component of the later-described gold-germanium (Au-Ge) alloy from harmfully affecting said semiconductor chip 1 as a P type impurity. Said nickel layer 5 is bonded to a lead frame 9 by a brazing layer 7 prepared from an alloy mainly consisting of gold and germanium (hereinafter referred to as "the alloy layer 7").

The conventional semiconductor device constructed as described above is generally received in a mold of, for example, synthetic resin (not shown). When, however, a semiconductor device of such construction is applied for long hours in an atmosphere of, for example, high humidity, moisture tends to seep into an interstice defined between said synthetic resin mold and semiconductor device. As a result, a local battery is likely to be produced between the nickel layer 5 and alloy layer 7. In such cases, the nickel layer 5 acts as a negative electrode, and the alloy layer 7 functions as a positive electrode. The nickel layer 5, now acting as a negative electrode, undergoes electrolytic corrosion and melts, probably resulting in the formation of a gap in part of the interface between said vanadium layer 3 and alloy layer 7 or giving rise to the brittle condition of the nickel layer 5 itself. When, therefore, the nickel layer 5 undergoes electrolytic corrosion, the semiconductor chip 1 tends to be dislodged from the lead frame 9. Further, when the lead frame 9 is applied as a collector electrode and the nickel layer 5 undergoes electrolytic corrosion, insufficient electrical connection results between the semiconductor chip 1 and lead frame 9, deteriorating the electrical property of the semiconductor device. For instance, the saturated voltage Vce (set) between the collector and emitter raises during the application of the semiconductor device, or its electric property falls off the prescribed initial level. Further, when the nickel layer 5 is subject to electrolytic corrosion, heat transmission between the semiconductor chip 1 and lead frame 9 falls (thermal conductivity decreases). In such cases, heat radiated from the semiconductor is not fully released due to the failure of not being sufficiently transmitted to the lead frame 9. The Au-Ge alloy needed as a brazing agent is extremely expensive because it mainly consists of gold and this has obstructed the reduction in cost for a semiconductor device.

This invention has been accomplished in view of the above-mentioned circumstances, and is intended to provide highly reliable semiconductor device which can be cheaply manufactured.

To attain the above-mentioned object, this invention provides a semiconductor device which comprises a semiconductor chip, at least one metal layer mounted on the bottom plane of the semiconductor chip, a lead frame, and a tin-copper alloy layer for brazing together the at least one metal layer and the lead frame.

This invention provides an inexpensive semiconductor device of high reliability which offers the advantages that regardless of the rigid condition in which the subject semiconductor device is applied for long hours, no local battery is created between the at least one metal layer and alloy layer; the semi-conductor chip does not fall off the lead frame; the subject semiconductor device does not deteriorate in electrical property; the saturated voltage impressed between the collector and emitter of the subject semiconductor device is not raised; the electrical property of the subject semiconductor device does not fall off the specified initial level; heat transmission between the semiconductor chip and lead frame does not decline; noticeable reduction is ensured in the cost of manufacturing a semiconductor device, and particularly the cost of the alloy layer; and the normal cost of a tin-copper alloy is lower than one tenth of that of the Au-Ge alloy.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a cross sectional view of a common semiconductor device;

Fig. 2 is a cross sectional view of a semiconductor device according to a first embodiment of this invention, showing one step of the sequential steps of its manufacturing; and

Fig. 3 is a cross sectional view of a semiconductor device according to a second embodiment of the invention, showing one step of the sequential steps of its manufacturing.

A description may now be made with reference to Figs. 1 and 2 of a semiconductor device according to a first embodiment of this invention. A semiconductor device embodying this invention is characterized in that the alloy layer 7 shown in Fig. 1 is prepared from a tin-copper alloy. A semiconductor device of such construction can be manufactured through the undermentioned steps.

A vanadium layer 3 is formed on the backside (which is bonded to a lead frame) of a semiconductor wafer before being divided as a semiconductor chip. This vanadium layer 3 is produced by the evaporation process with a thickness ranging, for example, between 30 nm and 70 nm. A nickel layer 5 is formed underneath said vanadium layer 3 by the evaporation process with a thickness ranging, for example, between 100 nm and 300 nm. This nickel layer 5 reduces the P type impurity effect executed on the

semiconductor chip 1 by the copper included in the above-described tin-copper alloy layer 7. The tin-copper alloy layer 7 is formed underneath said nickel layer 5 by evaporation process. And the tin-copper alloy layer 7 comprises 38 % to 92.4 % by weight of tin and copper as the remainder. This tin-copper alloy layer 7 is deposited with a thickness ranging between, for example, 0.5 μm and 10 μm. Tin and copper have substantial the same temperature under the same vapor pressure. For instance, when the vapor pressure stands at 0.1 Torr, the tin has a temperature of 1685 K and the copper has a temperature of 1690 K. Therefore, tin-copper alloy layer 7 which is deposited by the evaporation process has substantially the same composition as the tin-copper alloy used as a evaporation source. A semiconductor wafer on the backside of which aforesaid three layer 3, 5, 7 are mounted is divided into individual semiconductor chips by scribing. Thus is obtained a semiconductor chip of Fig. 2, on the backside of which the three layers 3, 5, 7 are deposited. The alloy layer 7 is pressed against a heated lead frame 9 to effect the melting of said tin-copper alloy layer, which is later cooled into the solid form. As a result, the nickel layer 5 deposited below the semiconductor chip 1 and lead frame 9 are secularly bonded together by the alloy layer 7. The subject semiconductor device having a construction shown in Fig. 1 is produced through the above-mentioned steps.

The manufactured semiconductor device was subjected to a pressure cooker test. This test was carried out by applying the normally molded semiconductor device embodying this invention to the following conditions for 300 hours:

Pressure	2 atmospheres
Humidity	100 %
Temperature	121° C

The semiconductor device of this invention proved by the test to offer the advantages that no electrolytic corrosion took place in the nickel layer 5, no change appeared in the property of said semiconductor device, and the semiconductor chip 1 did not fall off the lead frame 9.

The foregoing embodiment referred to the case where the alloy layer 7 comprised of 38 % to 92.4 % by weight of tin and copper as the remainder. The tin-copper alloy whose composition falls within the above range retains a liquid phase over a temperature of 415° C and melts at a relationly low temperature (415° C). Therefore, the semiconductor chip 1 can be easily fixed to the lead frame 9 and, moreover, is not-thermally effected. However, it will be noted that this invention is not limited to the above-mentioned embodiment. In so far as this invention goes, tin and copper are alloyed together in any optional proportions.

The aforementioned embodiment referred to the case where the alloy layer 7 comprises tin and copper. But this invention is not limited to this specific alloy. In other words, any alloy mainly comprising of tin and copper well serves the purpose, provided said alloy extents no harmful effect on the semiconductor chip 1. In other words, said alloy 7 may further comprise, for example, antimony (Sb), phosphorus (P), or bismuth (Bi). These metals reduce the effect of P type impurity exerted on the semiconductor chip 1 by the copper component of said alloy layer 7. When, therefore, the aforesaid vanadium layer 3 and the nickel layer 5 can fully eliminate the harmful effect of P type impurity exerted on the semiconductor chip 1 by the copper component of said alloy layer 7, it is not always necessary to add any of the above-listed metals: (Sb), (P) and (Bi).

In the foregoing embodiment, the alloy layer 7 was deposited with a thickness ranging between 0.5 μm and 10 μm. However, this invention is not limited to this. In other words, thickness of the alloy layer 7 may be selected optionally in consideration of the surface roughness of the lead frame 9.

The above-mentioned embodiment referred to the case where said alloy layer 7 was first formed and then fixed to the lead frame 9. However, this invention is not limited to this process. For instance, it is possible to deposit a gold layer 11 underneath the alloy layer 7 as shown in Fig. 3. The gold layer 11 prevents oxidation of the alloy layer 7. And later the gold layer 11 bonds together both semiconductor chip 1 and lead frame 9 by the same process as previously mentioned. During this step, the layers 7 and 11 melt, and later are cooled into a solid form. At this time, the gold constituting said layer 11 seeps into the alloy layer 7.

Throughout the foregoing embodiments, the vanadium layer 3 having a thickness ranging between 30 nm and 70 nm and the nickel layer 5 having a thickness ranging between 100 nm and 300 nm was deposited on the backside of the semiconductor chip 1. However, no limitation is imposed on the kind, number and thickness of metal layers deposited on the backside of the semiconductor chip 1. In other words, it is possible to apply any layer prepared from a known material provided it has a good brazing property, high conductivity and satisfactory thermal conductivity, exerts no harmful electric effect on the semiconductor chip 1, and prevents the copper component of the alloy layer 7 from undesirably affecting said semiconductor chip 1. Further, it is advised that the number and thickness of the above-mentioned metal layers, deposited on the backside of the semiconductor chip 1, be determined in consideration of the extent to which the copper component of the alloy layer 7 may affect the semiconductor chip. Further, the above-mentioned layers can be optimally formed, for example, by thermal deposition or plating.

CLAIMS

1. A semiconductor device which comprises:
a semiconductor chip;
at least one metal layer deposited on the

bottom plane of said semiconductor chip;

a lead frame; and

an alloy layer acting as a brazing agent for bonding together said at least one metal layer and lead frame, and wherein said alloy layer comprises tin and copper.

2. The semiconductor device according to claim 1, wherein said alloy layer comprises 38 % to 92.4 % by weight of tin and copper as the remainder.

3. The semiconductor device according to claim 1, wherein said alloy layer has a thickness ranging from 0.5 micron to 10 microns.

4. The semiconductor device according to claim 1, wherein said alloy layer further comprises antimony (Sb).

5. The semiconductor device according to claim 1, wherein said alloy layer further comprises phosphorus (P).

6. The semiconductor device according to claim 1, wherein said alloy layer further comprises bismuth (Bi).

7. The semiconductor device according to claim 1, wherein a gold layer is deposited on the plane, which is to be bonded to said lead frame, of said alloy layer; and later said alloy layer and gold layer are melted, thereby causing the molten gold to seep into said alloy layer.

8. The semiconductor device according to claim 1, wherein said at least one metal layer comprises:

a first metal layer deposited on the bottom plane of said semiconductor chip; and

a second metal layer formed of a different metal from that of said first metal layer and mounted thereon,

and said alloy layer bonds together said second metal layer and lead frame.

9. The semiconductor device according to claim 8, wherein said first metal layer is formed of vanadium and said second metal layer is prepared from nickel.

10. A semiconductor device, substantially as hereinbefore described with reference to Figs. 2 and 3 of the accompanying drawings.

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